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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/640,855	08/13/2003	Masayuki Ito	SHI-002	9146

7590 07/27/2006

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/640,855	ITO ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-9 and 13-17* is/are rejected.

7)☒ Claim(s) *3-5,10-12 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-18 are presented for examination. This office action is in response to the RCE filed on 6/6/2006.

Specification

2. The status of the referenced U.S. applications must be updated accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filed Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.) in the Related Applications section and in any other corresponding area in the specification, if any.

3. Again, all acronyms should be spelled out in the first use (.i.e. IP, page 6 line 14, UTLB, page 6 line 23, DTLB, page 6 line 24, etc).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 6-8, and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchihori U.S. Patent No. 4,961,135.

As to claim 1, Uchihori discloses the invention as claimed. Uchihori discloses a data processor, comprises a central processing unit (col. 4 lines 18-19), and an address translation unit (Fig. 9 Ref. 75) that receives a virtual addresses output (Col. 4 lines 10-34) from the central processing unit and outputs a physical addresses (col. 4 lines 17-20), wherein the address translation unit includes a first translation lookaside buffer (Fig. 9 Ref. 75A), a second translation lookaside buffer (Fig. 9 Ref 75 b), and a control circuit (Fig. 9 Ref. 77) for selecting one of the first and second translation lookaside buffers, wherein the control circuit selects one of the first and second TLBs to output a physical address based on stored enable information (col. 6 lines 24-27, Fig. 9 Ref. 82) wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the CPU (col. 6 lines 22-52).

As to claim 2, Uchihori further discloses wherein each of the first and second translation lookaside buffers has a plurality of entries for holding physical addresses associated with respective virtual addresses (Fig. 5 Ref. 31) respectively for performing the address translation, wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space, wherein the first translation lookaside buffer translates a virtual address of the first virtual

address space to the physical address, and wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address (Fig. 9 Ref. 75 and col. 6 lines 22-52).

As to claim 6, Uchihori further discloses wherein the control circuit decodes upper bits of a virtual address output from the central processing unit and selects one of the first and second translation lookaside buffers in accordance with a decode result (Fig. 9 Refs. 77 & 82 and col. 6 lines 22-52).

As to claim 7, Uchihori further discloses wherein the address translation unit further includes a selection circuit to which a first output of the first translation lookaside buffer and a second output of the second translation lookaside buffer are input, wherein the selection circuit selects one of the first and second outputs in accordance with a control signal of the control circuit (Fig. 9 Refs. 77 & 82 and col. 6 lines 22-52).

As to claim 8, Uchihori further discloses wherein the address translation unit further includes an address chop circuit (col. 6 lines 47-68) that fixedly forms a physical address from a virtual address when both of the first and second translation lookaside buffers are disabled (col. 9 lines 28-30, TLB miss reads on this limitation).

As to claim 13, Uchihori discloses the invention as claimed. Uchihori discloses a data processor, comprises a central processing unit (Col. 4 lines 18-20); and an address translation unit (Fig. 9 Ref. 75 and col. 6 lines 22-53) that receives virtual addresses output from the central processing unit and outputs a physical address (col. 4 lines 10-25), wherein the address translation unit includes a first translation lookaside buffer for performing address translation of a first virtual address space in the virtual addresses, a second translation lookaside buffer for performing address translation of a second virtual address space in the virtual addresses, and a control circuit (Fig. 9 Ref. 77) for selecting one of the first and second translation lookaside buffers in accordance with whether a virtual address output from the CPU is in the first virtual address space or the second virtual address space, wherein the control circuit selects one of the first and second TLBs to output a physical address based on stored enable information (col. 6 lines 24-27, Fig. 9 Ref. 82).

As to claim 14, Uchihori further discloses wherein each of the first and second translation lookaside buffers includes a plurality of entries for holding physical addresses respectively, associated with virtual addresses for performing address translation (Fig. 5 Ref 31 and Fig. 9 Ref. 75).

As to claim 15, Uchihori further discloses wherein the second translation lookaside buffer includes entries for an address translation miss handling routine of the first translation lookaside buffer, wherein the entries for the address

translation miss handling routine are disabled from rewriting (col. 6 lines 22-50, control bits V, M, VNA, VNB, MNA, MNA, and MNB read on this limitation).

As to claim 16, Uchihori discloses the invention as claimed. Uchihori discloses a design data module including information of a microprocessor module, comprises data for defining an address translation unit for receiving virtual addresses output (Col. 4 lines 10- 22) from a central processing unit and outputting physical addresses, wherein the address translation unit includes a first translation lookaside buffer (fig. 9 Ref 75a), a second translation lookaside buffer (Fig. 9 Ref 75b), and a control circuit (fig. 9 Ref. 77) for selecting one of the first and second translation lookaside buffers, wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the CPU (col. 6 lines 22-52), wherein the control circuit selects one of the first and second TLBs to output a physical address based on stored enable information (col. 6 lines 24-27, Fig. 9 Ref. 82).

As to claim 17, Uchihori further discloses wherein each of the first and second translation lookaside buffers has a plurality of entries for holding predetermined physical addresses associated with respective virtual addresses (Fig. 5 Ref. 31) for performing the address translation, wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space, wherein the first translation lookaside buffer translates a virtual address of the first virtual

address space to a physical address, and wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address (Col. 6 lines 24-26).

Alternatively

5. Claims 1-2, 6-7, 9, and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hussain U.S. Patent No. 6,205,531.

As to claims 1, 13, and 16, Hussain discloses the invention as claimed. Hussain discloses a data processor, comprises a central processing unit (Fig. 1 Ref 102), and an address translation unit (Fig. 2) that receives a virtual addresses output (Fig. 2 Ref. 208) from the central processing unit and outputs a physical addresses (Fig. 2 Ref 224), wherein the address translation unit includes a first translation lookaside buffer (Fig. 5 Ref. one of 500), a second translation lookaside buffer (Fig. 5 Ref. one of 5000), and a control circuit (Fig. 2 Refs. 214 203, and 206) for selecting one of the first and second translation lookaside buffers, wherein the control circuit selects one of the first and second TLBs to output a physical address based on stored enable information (col. 7 lines 1-5) wherein the address translation unit performs address translation in accordance with an area of a virtual address space of a virtual address received from the CPU (col. 7 lines 21-41).

As to claim 2, Hussain further discloses wherein each of the first and second translation lookaside buffers has a plurality of entries for holding

physical addresses associated with respective virtual addresses respectively for performing the address translation, wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space, wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to the physical address, and wherein the second translation lookaside buffer translates a virtual address of the second virtual address space to a physical address (Figs. 5 and 6).

As to claim 6, Hussain further discloses wherein the control circuit decodes upper bits of a virtual address output from the central processing unit and selects one of the first and second translation lookaside buffers in accordance with a decode result (col. 5 lines 1-5).

As to claim 7, Hussain further discloses wherein the address translation unit further includes a selection circuit to which a first output of the first translation lookaside buffer and a second output of the second translation lookaside buffer are input, wherein the selection circuit selects one of the first and second outputs in accordance with a control signal of the control circuit (Figs. 5 and 6).

As to claim 9, Hussain further discloses wherein a page size of the first translation lookaside buffer is different from a size of the second translation lookaside buffer (col. 7 lines 21-41).

As to claim 14, Hussain further discloses wherein each of the first and second translation lookaside buffers includes a plurality of entries for holding physical addresses respectively, associated with virtual addresses for performing address translation (Fig. 5).

As to claim 15, Hussain further discloses wherein the second translation lookaside buffer includes entries for an address translation miss handling routine of the first translation lookaside buffer, wherein the entries for the address translation miss handling routine are disabled from rewriting (col. 7 lines 12-20).

As to claim 17, Hussain further discloses wherein each of the first and second translation lookaside buffers (Fig. 5) has a plurality of entries for holding predetermined physical addresses associated with respective virtual addresses for performing the address translation (Fig. 5 Ref. 500), wherein the central processing unit is capable of accessing a first virtual address space and a second virtual address space included in the virtual address space, wherein the first translation lookaside buffer translates a virtual address of the first virtual address space to a physical address, and wherein the second translation

lookaside buffer translates a virtual address of the second virtual address space to a physical address (Figs. 5 and 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchihori U.S. Patent No. 4,961,135 in view of Hsu et al. (Hsu) U.S. Patent No. 5,526,504.

As to claim 9, Uchihori discloses the invention as claimed above. However, Uchihori does not specifically disclose wherein a page size of the first translation lookaside buffer is different from a size of the second translation lookaside buffer.

Hsu discloses wherein a page size of the first translation lookaside buffer is different from a size of the second translation lookaside buffer (col. 2 lines 40-58) for the purpose of supporting variable page sizes (abstract).

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate wherein a page size of the

first translation lookaside buffer is different from a size of the second translation lookaside buffer as taught by Hsu into the system of Uchihori for the advantages stated above.

Allowable Subject Matter

7. Claims 3-5, 10-12 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcome claim objections.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He

or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
571-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

HK
Primary Patent Examiner
July 24, 2006